

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: J.-S. Mok et al. Attorney Docket No: LEPA121687
Patent No: US 7435352 B2 Confirmation No.: 8329
Issued: October 14, 2008
Title: METHOD OF FORMING SOLDER RESIST PATTERN

REQUEST FOR CERTIFICATE OF CORRECTION

Seattle, Washington 98101

ATTN: CERTIFICATE OF CORRECTION BRANCH
COMMISSIONER FOR PATENTS:

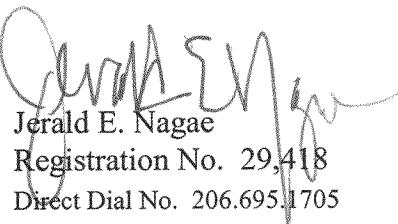
Enclosed is a Certificate of Correction, Form PTO-1050, for the above-identified U.S. Letters Patent. The error in the printed patent listed on the enclosed form occurred at the corresponding location in the application file listed below:

Column,	Line	Page,	Line
12 (Claim 14, line 15)	58	7 (Claim 15, (Amendment 2/15/2008)	3 line 9)

Since the Certificate of Correction is necessitated by a Patent and Trademark Office error, no fee is required.

Respectfully submitted,

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

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PATENT NO. : US 7435352 B2
 APPLICATION NO. : 10/677182
 ISSUE DATE : October 14, 2008
 INVENTOR(S) : J.-S. Mok et al.

It is certified that an error or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

<u>COLUMN</u>	<u>LINE</u>	<u>ERROR</u>
12	58 (Claim 14, line 15)	before "expose circuit patterns" delete "provide a solder resist pattern"

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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